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# High-Rate GaAs Epitaxial Lift-Off Technique for Optoelectronic Integrated Circuits

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In the epitaxial lift-off (ELO) technique, where a GaAs device structure is lifted off from a GaAs substrate using selective wet etching of an AlAs release layer, the etching rate of the AlAs layer is increased by a factor of ~8 by raising the etchant temperature to 40°C and adding a surfactant and an antifoaming agent to the etching solution. The mechanism of the high-rate lift-off process is discussed based on the solubility and the diffusion coefficient of the etching product ($H_2$) in the etching solution. Photoluminescence measurement results show that the quality of the GaAs film is not degraded by the high-rate lift-off process. A high-rate lift-off technique for large-diameter wafers is proposed.

KEYWORDS: epitaxial lift-off (ELO), surfactant, antifoaming agent, stirring, light interference effect, stress

## 1. Introduction

In recent years, extensive research has been carried out on optoelectronic integrated circuits (OEICs).[1–4] We have demonstrated the fabrication of OEICs on which optical waveguides, photodiodes, and CMOS circuits are integrated on Si circuit.[5] The final aim of the study is to realize an OEIC that includes light emitting diodes (LEDs) or laser diodes (LDs) (Fig. 1). We have already succeeded in fabricating and evaluating optical writing operations in the three-dimensional optically coupled common memory (3D-OCC memory), which consists of polished GaAs LEDs (120 $\mu$m in thickness) bonded on the Si memory circuit.[6] However, such thick LEDs are not suited to multilayer three-dimensional integration. Thin GaAs light emitting devices are necessary for an OEIC in which the LDs or LEDs are coupled with optical waveguides as shown in Fig. 1. New technologies for thinning the GaAs devices are strongly favored compared to polishing techniques, since the GaAs wafers are more fragile than Si.

The epitaxial lift-off (ELO) technique,[7,8] in which a GaAs device structure is lifted off from a GaAs substrate using selective etching of a thin AlAs release layer (10–50 nm), is of potential interest as a way to obtain high quality devices mounted on Si LSI, since the heteroepitaxial integration of III-V compound semiconductors still demands major research efforts to improve device quality. However, the etching rate of the AlAs release layer is very low (20 h for a 5×5 mm$^2$ sample), which is not practical. The HF concentration of the etchant for an AlAs release layer was below 10 wt.%, and the etchant was cooled at 0°C to suppress the generation of $H_2$ gas bubbles which are products of etching. The bubble generation disturbs etchant inflow and diffusion of the etching products through the narrow gap between the GaAs device layer and the substrate.

In this paper we report detection of an increase in the etching rate of the AlAs release layer by a factor of ~8 upon raising of the etchant temperature to ~40°C and addition of a surfactant and an antifoaming agent to the etching solution (diluted HF). Photoluminescence measurement results show that the GaAs crystal quality is not degraded during the high-rate lift-off process.

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## 2. Experimental

Figure 2 shows a sample structure used for the ELO. A GaAs/GaAlAs double-hetero-structure (DH, 2.95 $\mu$m thick) is grown on a GaAs substrate by molecular beam epitaxy (MBE) with a 10 nm AlAs release layer. The double-hetero-structure is built up by a 300 nm p-type ($3 \times 10^{18}$/cm$^3$) GaAs layer, followed by a 1000 nm p-GaAlAs ($5 \times 10^{17}$/cm$^3$) layer, a 400 nm p-GaAs ($1 \times 10^{17}$/cm$^3$)layer, a 1000 nm n-GaAlAs ($5 \times 10^{17}$/cm$^3$) layer and a 300 nm n-GaAs ($3 \times 10^{18}$/cm$^3$) layer. After coating of the sample surface with Apiezon wax (60 $\mu$m), the sample is cut to 3×3 mm$^2$ in size. Then the sample is dipped in the diluted HF (10 wt.% HF in $H_2O$) or the diluted HF with surfactant and antifoaming agent (10 wt.%, S10, Morita Chemicals Ltd.). The etching selectivity of AlAs with respect to GaAs in the diluted HF

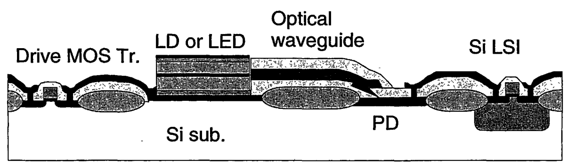


Fig. 1. Optoelectronic integrated circuits (OEICs) with optical waveguides, photodiodes, and LDs or LEDs on Si LSI.

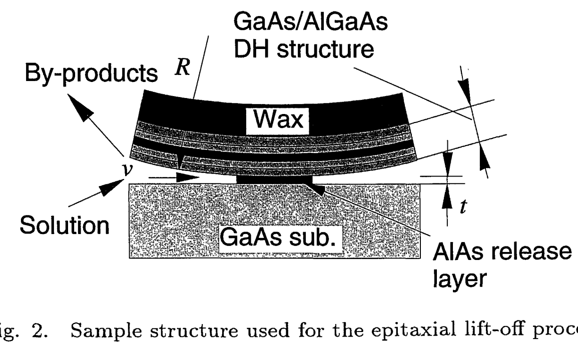


Fig. 2. Sample structure used for the epitaxial lift-off process.

is $\sim 10^7$.[9] The Apiezon wax coat induces strain in the sample which results in an increase in the gap between the GaAs device layer and the substrate as shown in Fig. 2. As a result, the etchant inflow and the removal of the etching products are enhanced. The temperature of the diluted HF solution is varied from 0 to 65°C. An automatic stirring machine is used to investigate the effect of stirring of the etching solution. The lateral etching rate of the AlAs layer is determined from the time needed to lift off the GaAs device layer from the substrate. For checking of the separation of the GaAs device layer from the substrate, ultrasonic vibration is applied to the etching solution for 15 sec every 30 min.

The crystal quality of the GaAs films before and after the lift-off process is evaluated by photoluminescence measurements using the pumping light of an $Ar^+$ laser (488 nm wavelength) at room temperature. The samples were mounted on a copper plate holder using an InGa alloy.

## 3. Results and Discussion

### 3.1 *AlAs etching rate in the lift-off process*

Figure 3 shows the lateral etching rate of the AlAs layer (10 nm in thickness) as a function of the temperature of the etching solution. Without surfactant and antifoaming agent (△), the etching rate decreases with increasing temperature. With increase in the temperature, the rate of generation of $H_2$ increases. In contrast, the solubility of $H_2$ in the solution decreases with increasing temperature. Thus $H_2$ bubbles are generated which obstruct inflow of the etchant and removal of the etching products through the narrow gap between the GaAs device layer and the substrate. Upon addition of the surfactant and antifoaming agent (○, ●), the etching rate increases ~8-fold as the temperature reaches ~40°C compared to 0°C. Stirring of the solution is more effective than not stirring it, except at around 40°C. Above 40°C the etching rate decreases with increasing temperature.

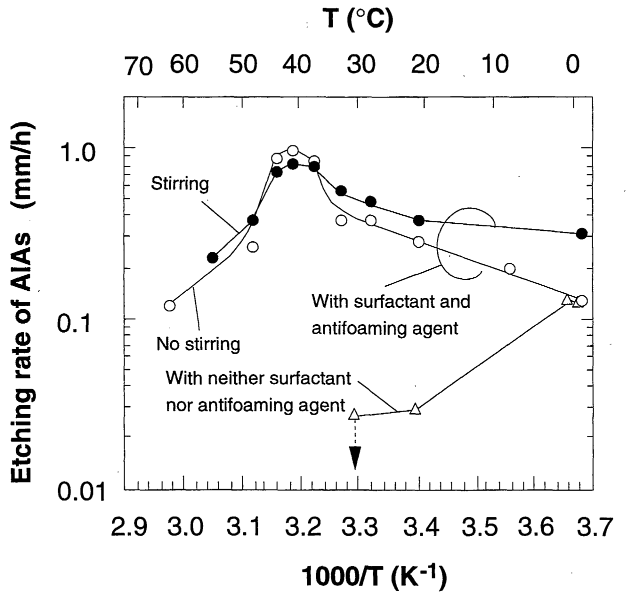


Fig. 3. AlAs selective etching rate as a function of temperature of the HF solution. The etching rate at 30°C in the solution with neither surfactant nor antifoaming agent is below 0.02 mm/h.

Figure 4 shows a model of AlAs selective etching during the ELO process. Theoretically the lateral etching velocity $v$ (cm/s) is given by the equations[7]

$$v = \frac{1}{3\pi\sqrt{(Rt/2)}} \cdot \frac{Dn}{N}, \tag{1}$$

$$D = D_0 \exp\left(-\frac{E_a}{kT}\right), \tag{2}$$

where $D$ denotes the diffusion coefficient of the dissolved $H_2$ in the solution, $n$ and $N$ are the molar concentrations of the dissolved $H_2$ and AlAs, respectively, $R$ is the radius of curvature of the GaAs device layer (see Fig. 2), $t$ is the thickness of the AlAs layer, $D_0$ is the diffusion coefficient for infinite temperature, $E_a$ is the activation energy, $k$ is the Boltzmann constant, and $T$ is the temperature of the HF solution. From these equations it is expected that the etching rate $v$ is considered to increase exponentially with increasing temperature. Here, $n$ varies only 27% in the temperature range of 0 to 65°C,[10] which is negligible compared with the exponential change in $D$. Addition of the surfactant results in an increase in $D_0$ and a change in $E_a$. Addition of the antifoaming agent results in an increase in $n$ through chemical reactions between generated $H_2$ and chemicals in the antifoaming agent. Therefore, the surfactant and the antifoaming agent are expected to act cooperatively in inducing the increase in the etching rate $v$.

The decrease in the etching rate with increasing temperature above ~40°C can be due to two effects: first, the hydrogen generation rate exceeds the capacity of the antifoaming agent, and secondly the wax induced strain is reduced by the softening of the wax (the gap in Fig. 2 becomes narrow).

### 3.2 *Photoluminescence measurement*

Figure 5 shows the photoluminescence (PL) spectra obtained for the DH layers before and after the lift-off process at room temperature. The luminescence from these layers is detected by a photomultiplier tube (PMT) in the wavelength range of 750 nm to 950 nm. For determination of the contributions from multiple internal reflectances within the multilayer stack, the emission spectra are taken at two angles of detection with respect to the sample surface normal. The emission spectrum for the DH before the lift-off process shows one broad

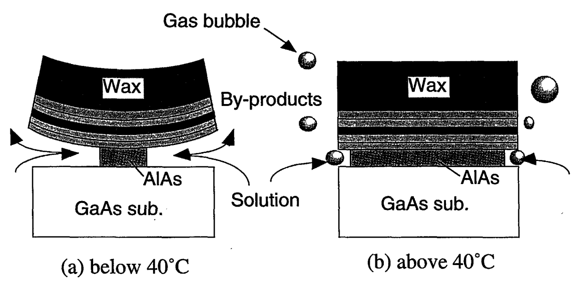


Fig. 4. AlAs etching model with HF solution temperatures of (a) below 40°C and (b) above 40°C.

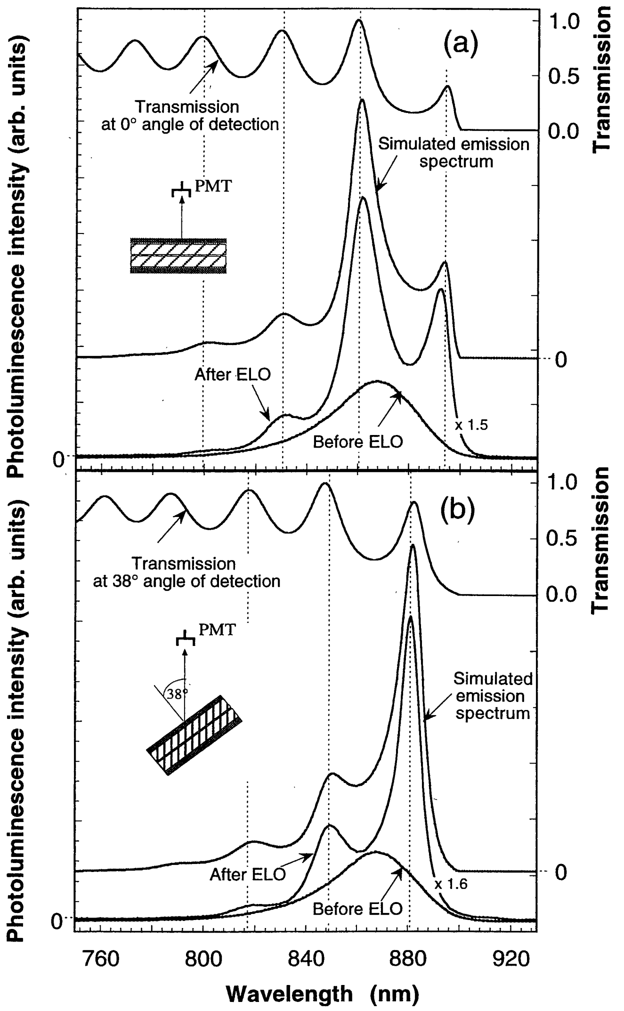


Fig. 5. Photoluminescence spectra of GaAs/GaAlAs (DH) structure (2.95 $\mu$m) before and after lift-off process using the pumping light of an $Ar^+$ laser (488 nm) at 297 K at two different angles of observation with simulated transmission and emission spectra: (a) Emission spectra taken at normal incidence before and after the lift-off process, and (b) emission spectra taken at an angle of observation at 38°. Also drawn are the calculated transmission at both angles of observation, as well as the simulated emission spectra with an assumed Gaussian emission distribution (see text).

emission peak at 873 nm, the shape of which can be fitted by three Gaussian curves with peak maxima at 875 nm, 865 nm and 855 nm with full width at half maxima (FWHMs) of 20 nm, 40 nm and 125 nm, respectively. After the lift-off process the emission spectrum for the multilayer stack taken at normal incidence consists of four maxima at 792 nm, 832 nm, 862 nm and 893 nm, respectively, as shown in Fig. 5(a). These maxima are shifted to higher wavelengths upon increase of the angle of detection. At a detection angle of 38°, the maxima are located at 881 nm, 850 nm and 820 nm.

For the simulation of the interference effect within the multilayer structure, the transmission of a five-layer stack (330 nm GaAs/955 nm GaAlAs/402 nm GaAs/955 nm GaAlAs/320 nm GaAs) was calculated as a function of wavelength for two angles of detection (0° and 38°). The luminescence that escapes from the GaAs surface region without interacting with the underlying multilayer stack is not included in the calculated transmission. The refractive index and absorption coefficient for the GaAs layers are taken from ref. 11 for nominally undoped GaAs. The GaAlAs layers were assumed to be transparent within the wavelength range of interest, with a refractive index of $n_{\mathrm{GaAlAs}} = 3.39$. Figures 5(a) and 5(b) also show the calculated transmission for this multilayer stack for both a 0° and 38° angle of detection. Since the emission is not constant over the whole wavelength range, the transmission spectra were multiplied by the emission spectrum for the GaAs DH before the lift-off process. The simulated emission spectra so calculated are also drawn for comparison and show excellent agreement with the experimental findings in Figs. 5(a) and 5(b).

The simulations also show that this interference phenomenon is strongly suppressed for a DH mounted on a GaAs substrate. The calculated transmission in this case is of the order of 70% with very weak undulations. With increasing wavelength above 880 nm, the transmission decreases rapidly. The decrease in the emission above 880 nm is in both cases, before and after the lift-off process, caused by interference phenomena in the DH and may mask the true position of the emission maxima in the wavelength range. Additionally, the absorption edge for the top, heavily doped p-type GaAs layer is most likely shifted towards higher wavelengths, which suggests that the absorption data used for undoped GaAs in the simulations may cause a sharp cut-off at the absorption edge around 880–890 nm. Both effects may contribute to the slightly reduced first maximum as it is observed in Fig. 5(a) for the simulated emission spectra.

The increase in emission intensity after the lift-off process can also be explained by the interference effect, since the transmission around the maxima in the thin lifted-off film exceeds 80 to 90%, whereas the transmission in the substrate-mounted DH stays around 70%.

The PL spectra for an undoped GaAs layer (3.5 $\mu$m thick) before and after the lift-off process are shown in Fig. 6. The intensities of the luminescence are the same, which indicates that no degradation effects occurred during the lift-off process. In this experiment no interference-induced modulation of the spectrum is observed due to the strong absorption in the thick GaAs layer. However, after the lift-off process the spectrum is split. This might be explained by stress induced during the lift-off process (GaAs film is bent by the stress of the Apiezon wax). These results indicate that no significant degradation occurs in the lifted-off film, since the light intensities before and after the high-rate ELO process are almost the same.

### 3.3 *Large area lift-off technique*

To extend this lift-off technique to large wafers, we propose a lift-off technique as outlined in Fig. 7. The sample wafer is structured with hatch pattern grooves and bonded to the sapphire (resistant to HF etching) substrate using resist. Artificial strain is applied onto the substrate via the holder using a screw. With a hatch pattern size of 3×3 mm$^2$, large wafers (for example 3 inches in diameter) can be lifted off within a practical etching

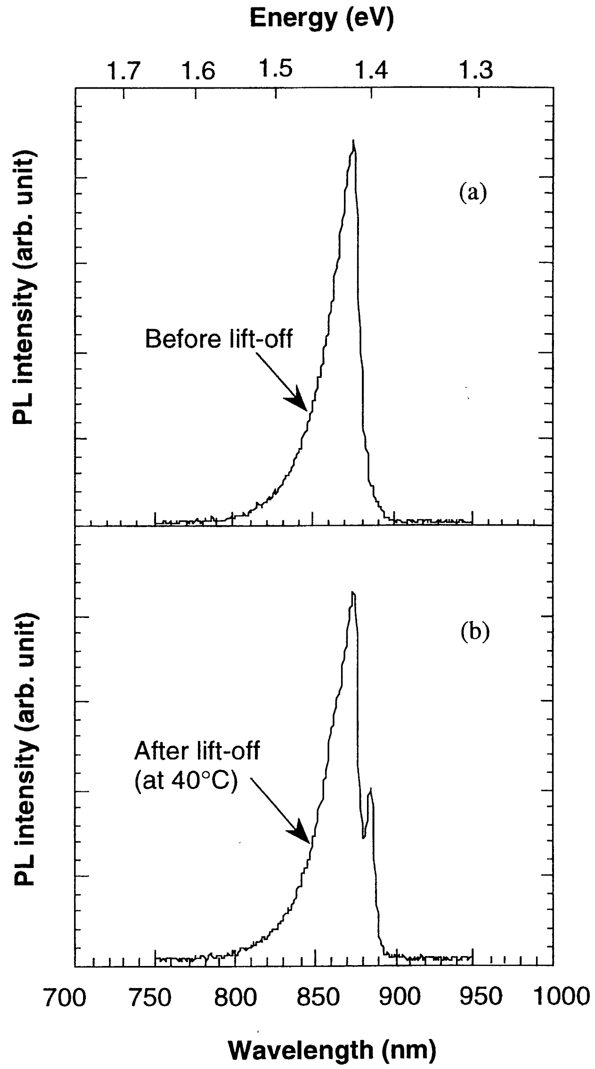


Fig. 6. Photoluminescence spectra of undoped GaAs layer (3.5 $\mu$m) excited with an $Ar^+$ laser (488 nm) at 297 K. (a) Before lift-off process. (b) After lift-off process.

time of 1.5 h using the developed etch technique.

## 4. Conclusions

High-rate (~8-fold) lift-off for GaAs devices has been achieved by adding a surfactant and an antifoaming agent to the diluted HF solution and raising the temperature to ~40°C. The crystal quality of the GaAs film is not degraded by this high-rate lift-off process. A new high-rate lift-off technique for large-diameter wafers is also proposed.

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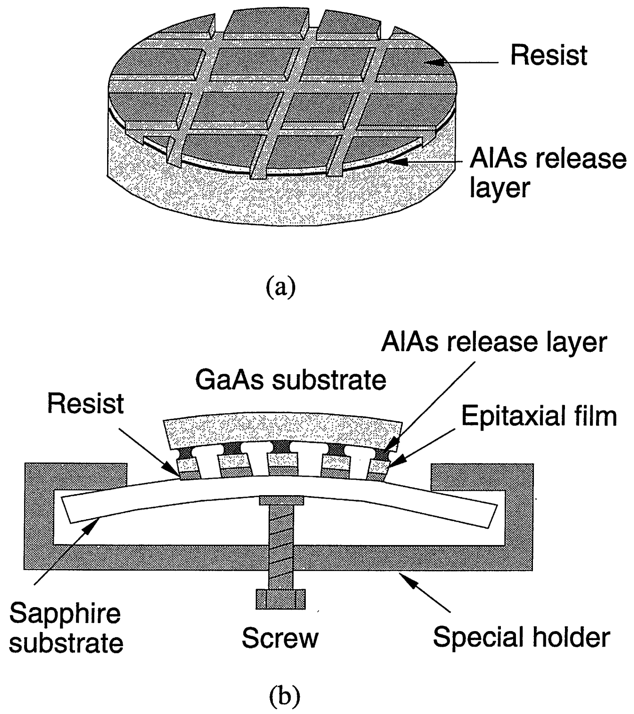


Fig. 7. Proposed enhanced large-area lift-off technique. (a) Sample wafer with hatch pattern grooves. (b) Cross section of sample with holder.

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