Heteroepitaxial growth of Si on GaP and GaAs surfaces by remote, plasma enhanced chemical vapor deposition

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Heteroepitaxial thin films of Si have been deposited onto GaP and GaAs substrates at low temperatures, <400 °C, by remote plasma-enhanced chemical vapor deposition. Cleaning and passivation of the GaP and GaAs surfaces, by *ex situ* wet chemistry, and *in situ* exposure to atomic-H at temperatures from 400 to 530 °C, were found to be critical in promoting epitaxial growth. The exposure to atomic-H was effective in removing surface oxides and hydrocarbon contamination. After the H-exposure, low energy electron diffraction (LEED) measurements revealed an ordered 1×1 structure for the GaP(111) surface, and a $c(8\times2)$Ga structure for the GaAs(100) surface. Heteroepitaxial films of Si have been deposited at temperatures from 300 to 400 °C and pressures between 50 and 500 mTorr, with the highest quality epitaxial growth proceeding on vicinal GaP(100) surfaces. In contrast, for the growth of Si on GaP(111) and GaAs(100) surfaces, LEED measurements indicate the onset of strain-induced disorder within the first few monolayers of the Si overgrowth.

I. INTRODUCTION

In previous investigations[1] we studied low temperature (<450 °C) Si homoepitaxial growth using the remote, plasma enhanced chemical vapor deposition (RPECVD) method. Specifically, it was found that the microstructure of thin Si films deposited on Si(100) surfaces depended strongly on process parameters such as total pressure and substrate temperature. Deposition "phase diagrams" were generated, as a function of pressure and temperature, and used to determine optimum growth conditions for low defect epitaxial growth. In this paper we continue that work with a focus on low temperature heteroepitaxial Si growth on GaP and GaAs surfaces.

As in the case for Si(100),[2,3] the nature of the pre-deposition surface treatment for both GaP and GaAs is crucial for promoting clean and defect-free surfaces prior to epitaxy. The use of atomic-H exposure for the preparation of Ga based III-V compound semiconductor surfaces has been studied by a number of researchers.[4,5] We have investigated the use of remote plasma generated atomic-H, for GaAs(100), GaP(111), and vicinal GaP(100) surfaces at temperatures ranging from 400 to 530 °C, as a means of surface contaminant removal and passivation. Unlike the strongly bonded oxides of Si, those of Ga, P, and As are found to be sufficiently weak to dissociate under the influence of atomic-H without inducing excessive surface structural damage.

Previously, Si molecular beam epitaxy (MBE) has been used to prepare Si/GaAs and Si/GaP heterostructures, at temperatures of 300 to 600 °C, for studies of their structural and chemical properties.[6,7] For processing temperatures below 500 °C, RPECVD has demonstrated a propensity for overcoming low thermal activation by providing an additional kinetic component to deposition reactions in the form of inert, activated plasma species.[1,8] In this paper, we report the use of this technique to study the feasibility of epitaxial growth of Si on GaAs and GaP surfaces. It is found that despite the small lattice mismatch between Si and GaP (~0.4% at 25 °C), the surface energetics by themselves are not enough to promote extended epitaxial growth unless stepped surfaces are used. For GaAs surfaces, where the Si lattice mismatch is much greater, ordered heteroepitaxial films do not propagate more than a few monolayers beyond the metallurgical interface.

II. SURFACE PREPARATION AND FILM DEPOSITION

A dual-function processing chamber in an ultrahigh vacuum-compatible (UHV) integrated processing system, described previously,[1] was used for both the pre-deposition surface preparation and Si thin film deposition. In an adjoining UHV chamber, surface chemical composition was monitored via Auger electron spectroscopy (AES) utilizing a single pass cylindrical mirror analyzer, while surface crystallinity was determined with a four grid, reverse-view LEED system.

Three different substrates were used in this study: *p*-type GaAs(100), *n*-type GaP(111), and vicinal *n*-type GaP(100), miscut 10°±0.5° toward ⟨011⟩. The *ex situ* cleaning steps for the GaAs consisted of a 30 s rinse in $NH_4OH:H_2O_2:H_2O$ (1:1:10), followed by 30 s in $NH_4OH:H_2O_2$ (1:10), ending with a 5 minute rinse in de-ionized, DI, H_2O, all performed at room temperature. For the GaP substrates, the procedure was a 60 s rinse in $NH_4OH:H_2O_2:H_2O$ (1:1:10), followed immediately by a 5 minute DI H_2O rinse, both at room temperature.

For experiments investigating the effect of atomic-H exposure, a 13.56 MHz rf H_2 plasma was ignited in a position remote (~30 cm) to, and facing away from, the substrate surface. Typical process conditions include a H_2 pressure of 10 mTorr, a rf power of 50 W, and substrate temperatures ranging from 400 to 530 °C. At a pressure of 10 mTorr, the

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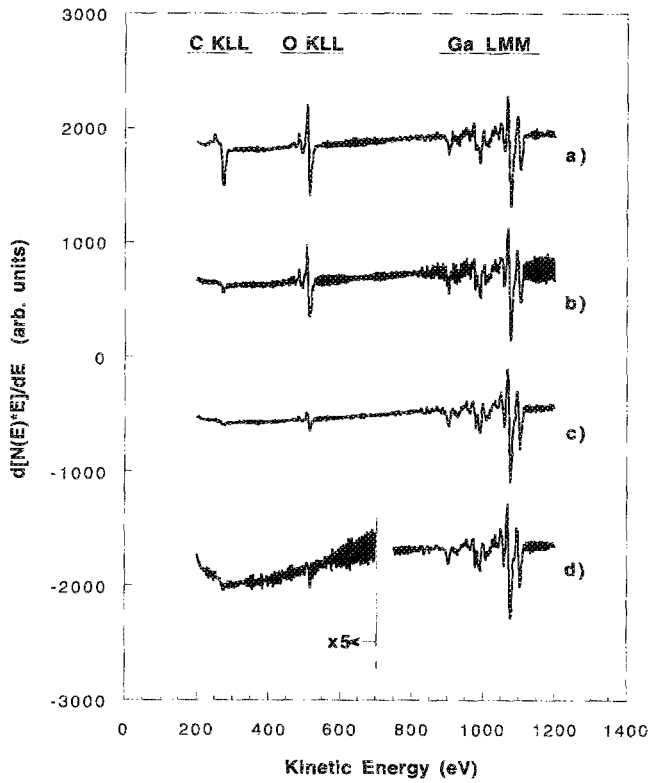

FIG. 1. Auger electron spectra for GaP(111) after: (a) wet chemical cleaning, (b) 530 °C anneal, for 20 min., (c) 2 min. H-plasma exposure, at 530 °C, and (d) 6 min. H-plasma exposure, at 530 °C.

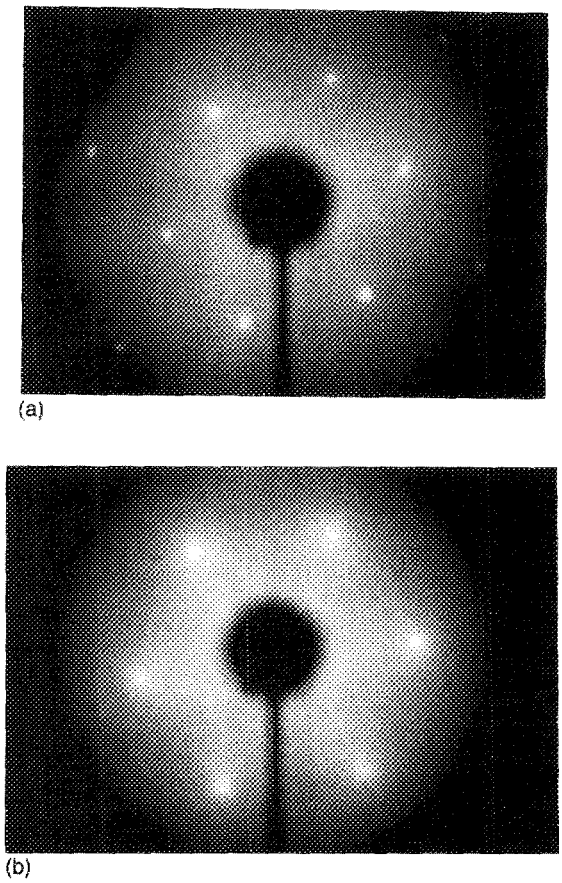

FIG. 2. (a) 1×1 LEED pattern for GaP(111) surface after exposure to atomic-H for 6 min. at 530 °C, beam energy: 86 eV. (b) 1×1 LEED pattern of 20 Å Si overlayer on GaP(111), beam energy: 60 eV.

balance of gas phase recombination and excitation reactions for atomic-H are shifted to allow a sufficient concentration of atomic-H to exist near the substrate; this drives surface reactions, even though the crystal surface faces away from the plasma source. Heating of the substrate is achieved through a bank of quartz halogen lamps directly irradiating the surface of interest.

Deposition of Si on both the GaAs and GaP surfaces was also achieved with a remote RF plasma process. In this process, deposition is accomplished by exciting a downstream-injected H_2/SiH_4 mixture with active species extracted from an upstream He plasma source. The deposition conditions include a rf power of 50 W, He flow of 200 sccm, H_2 flow of 25 sccm, and a dilute SiH_4:He (1:10) flow of 10 sccm. The distance of the substrate from the plasma source is nominally 25 cm. The critical parameters of temperature and pressure are maintained in the range of 300 to 400 °C and 50 to 500 mTorr, respectively.[1] All of the film thicknesses were determined by cross-sectional, high resolution transmission electron microscopy (HRTEM).

III. RESULTS AND DISCUSSION

A. Surface cleaning and passivation

The chemical consequences of atomic-H exposure on the wet chemically cleaned GaP(111) surface are shown in Fig. 1. After the *ex situ* cleaning step, the AES spectra reveal significant amounts of residual carbon and oxygen on the surface, presumably due to hydrocarbon contamination and native oxides, respectively. The GaP surface was then heated to 530 °C, and annealed for 20 minutes in a 10 mTorr H_2 ambient (50 sccm H_2 flow). The resulting AES spectrum indicates a significant reduction in the C *KLL* signal, a typical response to heating for physisorbed hydrocarbon species. Note that the O *KLL* signal is not significantly reduced, indicative of a more strongly bonded oxide compound on the surface.

After a 2 minute exposure to atomic-H at 530 °C, as indicated in Fig. 1(c), the O *KLL* peak is significantly reduced. This is attributed to the chemical reduction of native Ga–O and P–O bonds by activated H species.[4] For atomic-H exposures of up to 6 minutes, all but trace amounts of O and C are removed, thereby generating a relatively clean GaP(111) surface.

Figure 2(a) shows the LEED pattern for the clean GaP(111) surface after a 6 minute atomic-H exposure, at 530 °C. A distinct, three-fold, 1×1 surface symmetry, emulating that of the bulk structure, is observed. This result is similar to that reported by Lee *et al.*,[9] for GaP(111) surfaces that were cleaned by Ar ion bombardment and then annealed at 550 °C. The relatively bright background in the 1×1 LEED pattern of Fig. 2(a) is believed to be due to disorder brought on by the onset of surface etching by the atomic-H in areas where C and O have already been removed; this

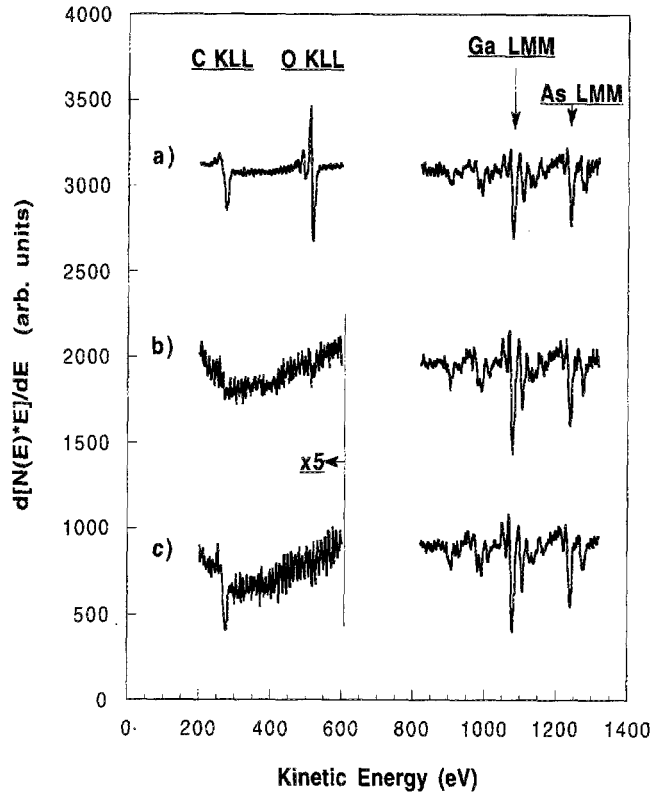

FIG. 3. AES spectra of the GaAs(100) surface after, (a) wet-chemical cleaning, (b) atomic-H exposure for 1 min. and, (c) atomic-H exposure for 20 min., both at 400 °C.

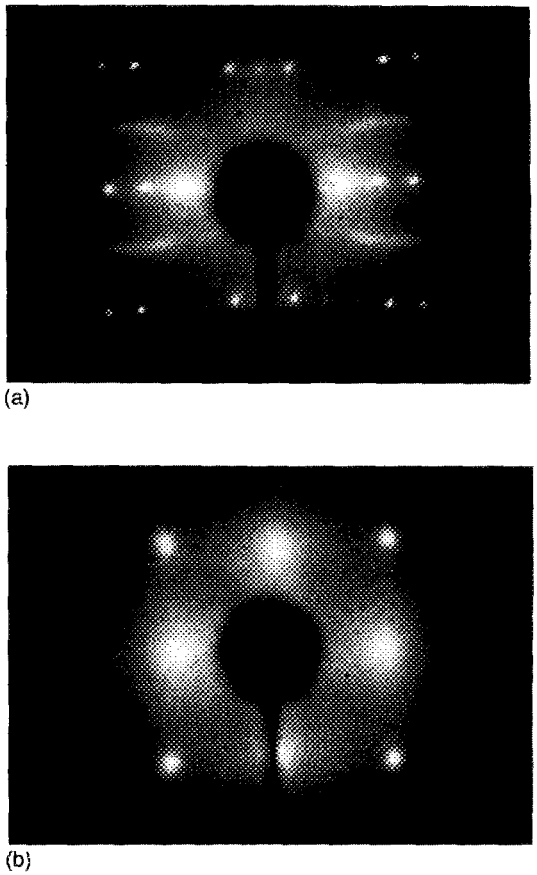

FIG. 4. (a) GaAs(100)-$c(8\times2)$Ga LEED pattern produced by exposure to atomic-H for 20 min. at 400 °C, beam energy: 49 eV. (b) 1×1 LEED pattern for a 10 Å Si overlayer, grown at 300 °C, beam energy: 65 eV.

process can lead to surface damage and the formation of undesirable surface electronic states.[4]

Similar experiments were performed on the vicinal GaP(100) substrates. AES spectra, taken under identical conditions of atomic-H exposure used for GaP(111), also indicate the effective removal of surface C and O. However, for the vicinal (100) surface, processing times of 15–20 minutes were necessary to achieve the same level of cleanliness that a 6 minute exposure produced on a (111) surface. This discrepancy can be understood in terms of more complex bonding arrangements at the steps on the vicinal (100) surface. This is a manifestation not only of the added complexity of exposed surface orbitals, but also on the possibility of strongly bonded O and C atoms at step and kink sites of the miscut surface. LEED patterns generated from these clean, vicinal GaP(100) surfaces exhibited no recognizable symmetry. It is believed that small, aperiodic terrace formation, along with process induced surface damage, both contribute to the lack of detection of a well ordered surface symmetry.

Figure 3 shows a typical AES spectra of a GaAs(100) surface under the influence of atomic-H exposure. As in the case for GaP, we see that the *ex situ* cleaned surface has a notable C and O presence. However, after only a 1 minute atomic-H exposure, at 400 °C, we detect virtually no surface C or O contamination. The ability to clean the GaAs surface in shorter times and at lower temperatures than a GaP surface, is a direct consequence of differences in the local bonding strength of the oxides of As and P. The energy, and hence stability, of the P–O bond is much greater than that of an As–O bond.[4,10] The relative advantage of this characteristic lies in the ability of the remote H-plasma process to clean the GaAs(100) surface more effectively, with less induced surface damage. This observation is reflected in the LEED pattern obtained for a GaAs(100) surface, and shown in the top of Fig. 4 after a 20 minute atomic-H exposure at 400 °C .

The LEED pattern recorded in Fig. 4(a) is identified as the GaAs(100)-$c(8\times2)$Ga surface. In this pattern, we see that the offset, fractional order spots representing the center, c, of symmetry are replaced with a continuous streak (indicative of some degree of surface disorder). Our identification of this Ga-terminated, centered 8×2 reconstruction was based on a measurement of the ratio of the 31 eV As *MVV* Auger peak height to the 55 eV Ga *MVV* peak height. A value for this ratio of 1.74 is found to be in exact agreement with the results of Drathen *et al.*,[11] for the $c(8\times2)$Ga surface. The tendency for the GaAs(100) to reconstruct, which was not seen for GaP(100), is attributed to the ease of removal of the less stable As-oxide, resulting in a cleaner, less damaged surface, with more long range order (due to its flatness). The fact that the surface is Ga-stabilized is consistent with previous studies that As–H is etched preferentially over Ga–H, As–H being volatile in vacuum.[12]

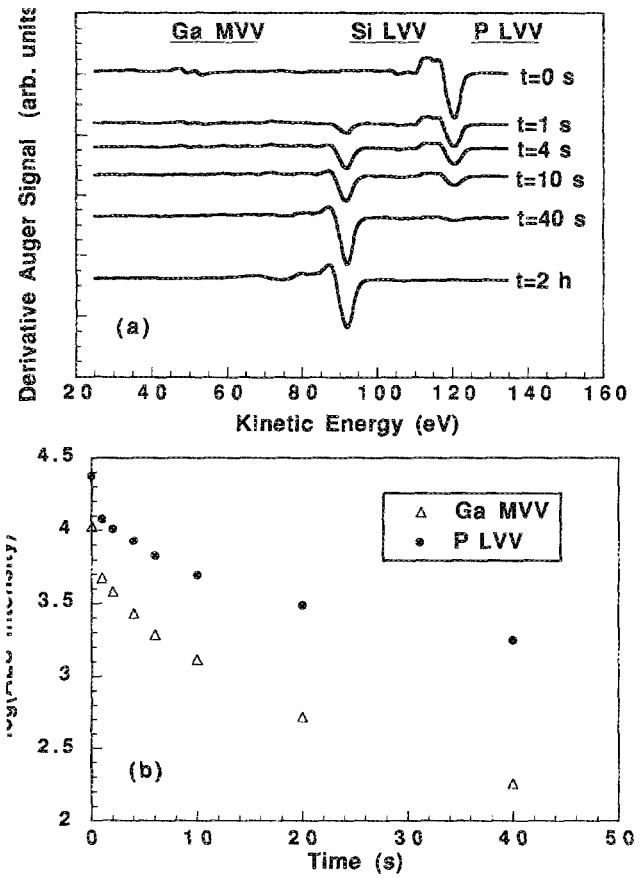

FIG. 5. (a) Auger electron spectra showing the evolution of Si coverage on vicinal GaP(100) for various deposition times. (b) Decay of the Ga *MNN* and P *LVV* signals with Si overlayer coverage. The growth temperature is 400 °C.

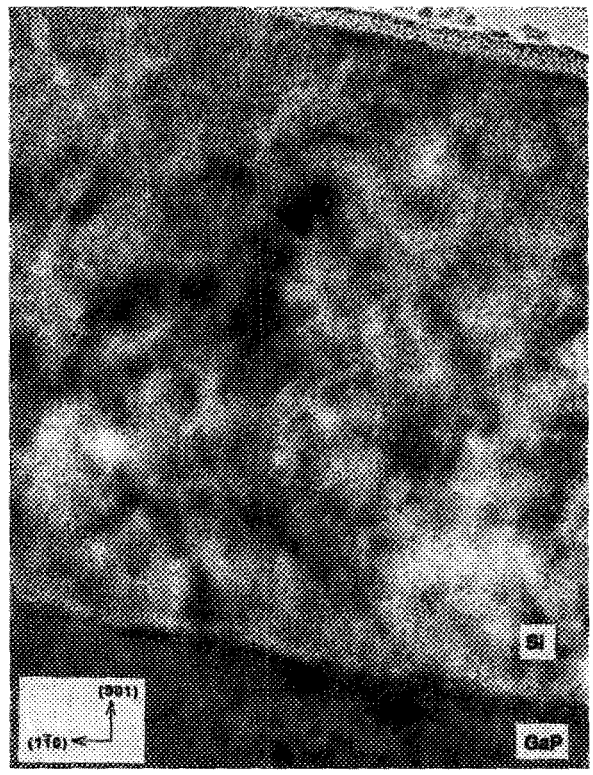

FIG. 6. Cross-sectional HRTEM image of a 775 Å Si film, deposited at 400 °C, on vicinal GaP(100), miscut 10°±0.5° toward ⟨011⟩.

B. Low temperature Si deposition

Using a deposition process compatible with low temperature processing provides a number of important advantages. Included among these is a reduction in impurity segregation. Both Ga and P are dopants in Si, and at processing temperatures above 700 °C, their solubilities are high enough to promote diffusion into the growing film. At processing temperatures below 400–500 °C, the problem of impurity segregation is severely curtailed, which not only allows for better control of electrical properties, but also affords the possibility of forming abrupt junctions.

For the vicinal GaP(100) surface, Si films were deposited at 400 °C and at a total pressure of 500 mTorr. Under these conditions, AES spectra were obtained over an energy range that included the Ga *MVV*, Si *LVV*, and P *LVV* peaks, as a function of deposition time [see Fig. 5(a)]. Figure 5(a) shows the evolution of the Si overlayer coverage as the substrate AES signal is attenuated by the presence of the growing film; the top spectrum, for $t=0$ s, is for the clean GaP(100) surface. A logarithmic plot of the peak-to-peak intensities of the Ga, Si, and P components, as a function of deposition time, indicates a nearly exponential decay of both the Ga *MVV* and P *LVV* substrate signals [see Fig. 5(b)]. This type of behavior is characteristic of a two dimensional growth mode, and there is no evidence of island formation. This result is in agreement with the data of de Jong *et al.*,[6] for Si MBE overlayer coverage on GaP(100). The fact that the substrate AES signals did not fit a perfect exponential decay, dropping off somewhat quicker than an exponential would warrant, may be an indication of Si alloy formation at the initial stages of the deposition process.

The bottom spectrum in Fig. 5(a) shows the surface composition of a 300 Å Si film. It shows no evidence of Ga or P segregation to the growth surface, which was at 400 °C. This is in contrast to the results of de Jong, *et al.*,[6] where Ga was detected at the surface of Si films as thick as 1100 Å, grown at 450 °C. We intend to perform secondary ion mass spectrometry (SIMS) analysis of our films in order to confirm the AES results.

Figure 6 is a cross-sectional HRTEM micrograph of a 775 Å Si film, deposited on the stepped GaP(100) surface, at a temperature of 400 °C and a total pressure of 50 mTorr. The image indicates a heteroepitaxial Si film of high quality, with no evidence of misfit slip dislocations propagating in the bulk structure. LEED patterns taken from the surface of the same film, immediately after deposition, indicated a fairly well ordered Si(100)-2×1 reconstructed surface, which was slightly streaked along the ⟨01⟩ direction, which is the result of surface steps.

For the GaP(111) surface, LEED analysis of Si films deposited under a range of pressures and temperatures indicated the emergence of crystal defects, and subsequently sur-

face disorder, after only a few monolayers of growth. For the simplest case of strain relief accommodated by slip dislocations in the interface plane, after Matthews and Blakeslee,[13] we have conservatively estimated the critical thickness, h_c, for the onset of defect generation, to be approximately 150 Å for the Si on GaP system. The bottom LEED pattern shown in Fig. 2 shows the 1×1 surface structure of a 20 Å Si film on GaP(111), grown at 300 °C and 500 mTorr. Compared to the LEED pattern for the clean GaP(111) surface [Fig. 2(a)], we see broadening of the diffraction spots and a loss of contrast, both indicative of the onset of surface disorder. Since the critical thickness is much greater than 20 Å, we conclude that this disorder may be the result of surface diffusion limits.

Similar to the growth mode study carried out from the data in Fig. 5 for vicinal GaP(100), we also analyzed the decay of the Ga *MVV* and P *LVV* peaks as a function of Si overlayer coverage for GaP(111). Once again, their nearly exponential decay indicated a two dimensional mode of growth. Assignment of the growth mode as layer-by-layer would assume sufficient surface mobility of deposition species to propagate the epitaxial film out to its critical thickness for misfit strain relief. We therefore conclude that, due to low deposition species surface mobility, a layer-by-layer growth mode is not attained, leading to the premature onset of crystal disorder.

For the stepped GaP(100) surface, Fig. 6 shows that quality single crystal growth can be propagated to thicknesses of at least 775 Å. Although the surface mobilities of deposition species may be higher for the (100) surface than the (111) surface, we attribute most of this behavior to surface step kinetics. Close scrutiny of the HRTEM micrograph indicates the terrace sizes to be in the range of 50–60 Å. Migration of deposition species to stable bonding sites at steps and kinks on the surface is therefore more probable, which leads to much improved crystallinity.

Figure 4 (b) shows the 1×1 LEED pattern generated by a 10 Å Si overlayer on GaAs(100). As in the case for Si on GaP(111), this pattern indicates the onset of surface disorder in the initial stages of growth. For GaAs, however, misfit strain relief is a much greater factor than for the Si/GaP system. At room temperature, the misfit for the Si/GaAs system is ~3.9 %. Calculation of the critical thickness, for the case of strain relief in the interface plane,[13] yields h_c to be less than 20 Å. This high degree of misfit strain then couples with low surface mobilities to generate defects after the first few monolayers of growth.

IV. CONCLUSIONS

We have demonstrated growth of high quality Si epitaxial layers on stepped GaP(100) surfaces, at low substrate temperatures. The advantages of low temperature processing of these heterostructures, decreased impurity segregation and abrupt junctions, have been realized. At the same time, it is observed that for flat GaP(111) surfaces, kinetic barriers to surface diffusion inhibit the propagation of defect free epitaxial Si films, grown at 300–400 °C. Also, the use of remote plasma generated atomic hydrogen has been shown to be an effective technique for pre-deposition cleaning and passivation of GaP and GaAs surfaces.

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